UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,699	07/02/2001	Dong-woo Lee	9898-176	2435

20575 7590 01/22/2008
MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2628	
MAIL DATE	**DELIVERY MODE**
01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/898,699	LEE ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-12,14,15,17,18,20,24-27 and 32-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-12,14,15,17,18,20,24-27 and 32-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 29, 2007 has been entered.

Response to Arguments

2. Applicant's arguments, see p. 11-16, filed October 29, 2007, with respect to rejection(s) of claim(s) 1, 3, 5-12, 14, 15, 17, 18, 20, and 24-27 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shiraishi (US005828378A).

3. As per Claim 1, Applicant argues new external depth data of Deering (US005544306A) is not transferred via the connecting line, into memory cell array. New data N[31..0] stops at Pixel ALU 58. Signal carried on output write port 202 is a blend of internal pixel value, new external pixel values, and other information. Signal carried on write port 202 is not new data N[31..0]. Even though write port 202 connects Pixel ALU 58 to pixel buffer 56, new data N[31..0] is not transferred via write port 202 into pixel buffer 56 (p. 11).

In reply, Examiner agrees. But, new grounds of rejection are made in view of Shiraishi.

4. As per Claim 3, Applicant argues that if the INVALID bit of Dowdell (US005301263A) is the first control signal, then the first control signal is not received originally from the memory controller. Rather, the INVALID bit is received originally from memory (p. 15).

In reply, Examiner points out Dowdell describes "INVALID byte is written to memory and the desired INVALID byte is then read from memory" (c. 4, ll. 15-20). As shown in Fig. 1, memory controller 122 writes data to memory 124. So, INVALID bit that is written to memory is received originally from memory controller.

5. As per Claim 5, Applicant argues that it is unclear how the first control pin can be both the PA_PASS_IN signal and the separate PA_PASS_OUT signal of Deering (p. 16).

In reply, Examiner points out that Deering shows in Fig. 8 that both the PA_PASS_IN signal and the PA_PASS_OUT signal are transmitted through first control pin 178.

6. Applicant argues prior art fails to teach each of the elements of Claims 32-35 (p. 16).

Examiner has made new grounds of rejection in view of Ryherd (US004970499A).

Claim Rejections - 35 USC § 103

7. Text of Title 35, U.S. Code 103(a) not included action can be found in prior action.

8. Claims 1, 6, 7, and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deering (US005544306A) in view of Shiraishi (US005828378A).

9. As per Claim 1, Deering teaches memory device (71, Fig. 1) for use with memory controller (70; c. 5, ll. 66-c. 6, ll. 1), memory device having memory cell array (56, Fig. 2; c. 7, ll. 27-30) adapted to store internal depth data of object (c. 8, ll. 30-34; c. 15, ll. 56-61; c. 16, ll. 60-62); compare circuit (235, Fig. 8; c. 15, ll. 56-61); line (204, Fig. 2) connecting compare circuit to memory cell array (c. 15, ll. 24-26, 46-49); and data modifying circuit (58) distinct from memory controller, data modifying circuit including compare circuit (c. 15, ll. 11-13) and being adapted to receive corresponding new external depth data of object from memory controller (c. 15, ll. 56-61; c. 16, ll. 62-67; c. 5, ll. 66-c. 6, ll. 1), compare new external depth

data with internal depth data (c. 15, ll. 56-61), and transfer external depth data, into memory cell array, depending on result of comparison, if external depth data is transferred, over-write internal depth data in memory cell array with transferred external depth data, and output to memory controller a status signal (c. 17, ll. 1-10; c. 5, ll. 66-c. 6, ll. 4; c. 6, ll. 53-62). Deering teaches two lines (202, 204) connecting data modifying circuit 58 to memory cell array 56 for transferring depth data. One connecting line transfers depth data from memory cell array 56 to data modifying circuit 58, which is connecting line 204 (c. 8, ll. 1-5, 12-14; c. 15, ll. 24-26, 46-49). Compare circuit 235 enables other connecting line to transfer external depth data from data modifying circuit to 58 memory cell array 56, which is connecting line 202 (c. 8, ll. 65-67; c. 17, ll. 1-10). Connecting line 204 is for transferring depth data from memory cell array 56 to compare circuit 235 (c. 15, ll. 24-26, 46-49).

However, Deering teaches external depth data undergoes blending of internal pixel values, new external pixel values and other information, and this blend is transferred into memory cell array (c. 6, ll. 31-34), and does not explicitly teach transferring external depth data, via line connecting compare circuit to memory cell array, into memory cell array. However, Shiraishi teaches compare circuit (35, Fig. 14) that compares new external depth data with internal depth data, transfer external depth data, via connecting line, into new z data register 36, and then from new z data register 36 into memory cell array 4a, depending on result of comparison (Fig. 14, c. 8, ll. 38-47). Deering teaches pixel ALU 58 transfers blend that is result of new external depth data, via connecting line, into memory cell array (c. 6, ll. 31-34). So, device of Deering can be modified so new external depth data is transferred, via connecting line, into memory cell array without having to undergo blending operation, as suggested by Shiraishi.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Deering to include transferring external depth data, via line connecting compare circuit to memory, into memory because Shiraishi suggests storing new external depth data before using depth data to perform operations is advantageous because new external depth data can be retrieved from memory to perform several different operations (c. 15, ll. 21-32).

10. As per Claims 6-7, Deering does not teach register explicitly for purpose of storing received new external depth data, and external depth data is written, via connecting line, into memory cell array. But, Shiraishi teaches data modifying circuit includes register (36, Fig. 14) for storing received new external depth data, compare circuit (35) is adapted to compare stored new external depth data with internal depth data, and adapted to write external depth data, via connecting line, into the register 36 and from register 36 into memory cell array 4a depending on result of the comparison (c. 8, ll. 38-47). Deering teaches pixel ALU 58 transfers blend that is result of new external depth data, via connecting line, into memory cell array (c. 6, ll. 31-34). So, Deering can be modified so new external depth data is transferred, via connecting line, into memory cell array without having to undergo blending operation, as suggested by Shiraishi.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Deering to include register explicitly for purpose of storing received new external depth data as suggested by Shiraishi because it provides for efficient data processing as z values are updated only if they are determined to be updated and unnecessary processing steps are eliminated resulting in processing efficiencies. Advantages of having external depth data written, via connecting line, into memory cell array were discussed for Claim 1.

11. As per Claim 24, Deering teaches first control pin (PA_PASS_IN, PA_PASS_OUT, 178, Fig. 8) that directly connects compare circuit (235) to memory controller (70, Fig. 1; c. 16, ll. 39-42; c. 17, ll. 1-10; c. 5, ll. 66-c. 6, ll. 4, c. 6, ll. 53-62), as shown in Fig. 8. Deering teaches FBRAM chip 71 provides one set of pixel port control input/output interface pins 114 for accessing pixel buffer 56 via compare circuit 58 (c. 9, ll. 51-57). So, Deering teaches 114 refers to pixel port control input/output interface pins, and since all control lines go through 114, this means control pins 114 directly connect compare circuit 58 to memory controller 70.

12. As per Claim 25, Deering teaches 1st control pin is adapted to receive 1st control signal (PA_PASS_IN) from memory controller (70, Fig. 1) and to output 1st status signal (PA_PASS_OUT) to memory controller (c. 17, ll. 1-10; c. 5, ll. 66-c. 6, ll. 4, c. 6, ll. 53-62), as shown in Fig. 8. Deering teaches FBRAM chip 71 provides 1 set of pixel port control input/output interface pins 114 for accessing pixel buffer 56 via compare circuit 58 (c. 9, ll. 51-57). So, Deering teaches 114 refers to pixel port control input/output interface pins, and since all control lines go through 114, this means control pins 114 directly connect compare circuit 58 to memory controller 70.

13. As per Claim 26, Deering teaches 2nd control pin that directly connects compare circuit (58, Fig. 4; c. 8, ll. 30-34) to memory controller (70, Fig. 1; c. 6, ll. 53-62; c. 11, ll. 8-15), as shown in Fig. 4. Deering teaches FBRAM chip 71 provides 1 set of pixel port control input/output interface pins 114 for accessing pixel buffer 56 via compare circuit 58 (c. 9, ll. 51-57). So, Deering teaches 114 refers to pixel port control input/output interface pins, and since all control lines go through 114, this means control pins 114 directly connect compare circuit 58 to memory controller 70.

14. As per Claim 27, Deering teaches second control pin is adapted to receive second control signal from memory controller (70, Fig. 1) and to output second status signal to memory controller (c. 6, ll. 53-62; c. 11, ll. 8-15), as shown in Fig. 4.

15. Claims 3, 5, 8-12, 14, 15, 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deering (US005544306A) and Shiraishi (US005828378A) in view of Dowdell (US005301263A).

16. As per Claim 3, Deering and Shiraishi are relied upon for teachings as discussed above relative to Claim 1. Deering teaches first control pin for receiving first control signal originally from memory controller (70, Fig. 1; PA_PASS_IN signal, c. 15, ll. 56-61; c. 17, ll. 2-10; c. 5, ll. 66-c. 6, ll. 4; c. 6, ll. 53-62), as shown in Fig. 10; and control circuit for transmitting external depth data to memory cell array (56, Fig. 2; c. 8, ll. 30-34; c. 15, ll. 56-61; c. 16, ll. 62-67).

However, Deering and Shiraishi do not teach bypassing data modifying circuit depending upon state of 1st control signal (81E, Fig. 9). Specification describes bypassing data modifying circuit depending as instant where depth compare writing is not going to occur (p. 5, ll. 9-21). Dowdell teaches similar process as follows in that incoming z-buffer address, new z-value are given as entry into FIFO 102. Controller 112 has to act on incoming pixel address to update new z-value, if necessary. Dowdell makes use of INVALID bit to validate new z-value to be written to memory (c. 4, ll. 3-67). Most significant, middle significant, and least significant bytes of old 24 bit z-values, R1, R2 and R3 and corresponding bytes of new 24 bit z-value denoted by W1, W2 and W3 and comparison is performed between R1 and W1 and if R1>W1, as determined by comparator 114, Fig. 2, then it is determined entire 24 bit old z-value is greater than entire 24 bit new z-value and consequently entire 24 bit new z-value consisting of W1, W2 and W3 must be

written to memory 124; however, if R1<= W1, then old 24 bit z-value is less than new 24 bit z-value, indicating new value should not be written to memory and in this case, updating operation is terminated immediately. Other comparisons between R2-W2; R3-W3 are detailed and termination of updating operation is detailed based on comparisons (c. 4, ll. 45-67; c. 5, ll. 1-55). Thus INVALID bit state is signal which then determines bypassing of update operations.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Deering and Shiraishi to include bypassing data modifying circuit depending upon state of first control signal as suggested by Dowdell because it results in conserving computing resources as no comparison has to take place.

17. As per Claims 5, 18, and 20, Deering teaches status signal is output through first control pin (c. 17, ll. 3-5). Deering shows in Fig. 8 both PA_PASS_IN signal and PA_PASS_OUT signal are transmitted through first control pin 178.

18. As per Claim 8, Deering teaches compare circuit (235, Fig. 8; c. 16, ll. 48-42) adapted to output status signal to memory controller (70; c. 17, ll. 1-5; c. 5, ll. 66-c. 6, ll. 4; c. 6, ll. 53-62).

19. As per Claims 9-11, Deering is silent about wherein compare circuit compares internal depth data with stored external depth in units of X bits/NX bits when second control signal is in non-active/active state. However, Dowdell teaches making use of an INVALID bit that indicates for particular pixel whether or not corresponding z-value memory location has valid z-value stored in it, with value of '0' indicating that it does and value of '1' indicating that it does not. Further, Dowdell teaches most significant, middle significant and least significant bytes of old z-value and new z-value being compared, and this it does not by processing all bits at once. Figure the MSB are compared, then middle significant and then least significant bytes and avoids

unnecessary processing using this logic (c. 4, ll. 40-67; c. 5, ll. 1-55) and INVALID bit (c. 4, ll. 3-10), providing valid status for a z-value at particular memory location.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Deering so compare circuit compares internal depth data with stored external depth in units of X bits/NX bits when second control signal is in non-active/active state as suggested by Dowdell because it results in efficient processing of z-values in comparator circuit.

20. As per Claim 12 and 17, Deering teaches processing depth data of object (c. 8, ll. 32-34) in memory device (71, Fig. 1) controlled by memory controller (70; c. 5, ll. 66-c. 6, ll. 1), comprising receiving external depth data of object from memory controller (c. 15, ll. 56-61; c. 16, ll. 62-66; c. 5, ll. 66-c. 6, ll. 1); storing received external depth data (c. 8, ll. 30-34); receiving 1st control signal from memory controller through 1st control pin distinct from memory controller (PA_PASS_IN, c. 15, ll. 56-61; c. 17, ll. 3-7; c. 5, ll. 66-c. 6, ll. 4; c. 6, ll. 53-62), as shown in Fig. 10; receiving stored external depth data and corresponding internal depth data stored in memory cell array (56, Fig. 2) at compare circuit (235, Fig. 8; c. 15, ll. 11-13; c. 15, ll. 56-61; c. 16, ll. 60-62) that is distinct from memory controller and connected via line (204, Fig. 2) to memory cell array (c. 15, ll. 24-26, 46-49) comparing, received data, writing from compare circuit, external depth data over corresponding internal depth data in memory cell array depending on result of comparison (c. 17, ll. 1-10); and receiving 2nd control signal from memory controller through 2nd control pin distinct from memory controller (c. 6, ll. 53-62), as shown in Fig. 4. Deering teaches 2 lines (202, 204) connecting data modifying circuit 58 to memory cell array 56 for transferring depth data. One connecting line transfers depth data from memory cell array 56 to data modifying circuit 58, which is connecting line 204 (c. 8, ll. 1-5, 12-14; c. 15, ll.

24-26, 46-49). Compare circuit 235 enables other connecting line to transfer external depth data from data modifying circuit to 58 memory cell array 56, which is connecting line 202 (c. 8, ll. 65-67; c. 17, ll. 1-10). Connecting line 204 is for transferring depth data from memory cell array 56 to compare circuit 235 (c. 15, ll. 24-26, 46-49).

But, Deering does not explicitly teach transferring external depth data, via line connecting the compare circuit to memory cell array, into memory cell array. However, Shiraishi is used to teach this limitation, as discussed in the rejection for Claim 1.

But, Deering and Shiraishi do not teach determining state of control signal whether active or inactive and comparing internal/external depth data in units of X/NX bits; outputting status signal indicating NX bits of internal depth have been modified. But, Dowdell teaches INVALID bit which is similar to control signal with active or inactive states, in that INVALID bit for particular pixel indicates whether or not corresponding z-value memory location has a valid z-values stored in it. Dowdell does 24 bit bits processing for comparing not at once, instead it does so based on MSB-LSB comparison thus avoiding unnecessary comparison steps (c. 4, ll. 5-67; c. 5, ll. 1-55). Dowdell does reporting of comparison bits and their modification, if carried out, as indicated by "done" state of Fig. 2.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Deering and Shiraishi to include determining state of control signal whether active or inactive and comparing internal/external depth data in units of X/NX bits; and outputting status signal indicating NX bits of internal depth have been modified as suggested by Dowdell because it provides a more efficient z-value comparison logic.

21. As per Claim 14, it is similar in scope to Claims 6-7, so is rejected under same rationale.

22. As per Claim 15, Deering does not teach writing external depth data takes place if comparison yields external depth data is larger than internal depth data. However, Dowdell teaches bytes R1, R2, and R3 of old z-values and W1, W2, and W3 of new z-values (c. 4, ll. 45-50) and comparison is performed between R1 and W1 and if R1>W1, then it is determined old z-value is greater than new z-value and consequently new z-value is written to memory 124 (c. 5, ll. 5-10). This would be obvious for the same reasons given in the rejection for Claim 3.

23. Claims 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryherd (US004970499A).

24. As per Claim 32, Ryherd teaches method for processing depth data of object in memory device controlled by display processor (c. 2, ll. 34-41). Fig. 6 shows graphical representation of operation of display processor in terms of utilization of clock cycles, and Fig. 6 shows six clock cycles, and indicates there are more than six clock cycles by the "etc." So, method comprises generating at least seven clock cycles. Display processor activates reading of data by read operation (c. 2, ll. 41-46), and this is considered to be activate command. Fig. 6 shows read operation is responsive to first clock cycle. So, activate command is received from display processor responsive to 1st of at least 7 clock cycles. Display processor receives external depth data using read operation, then performs compare operation between external depth data and depth of old pixel data and if appropriate, will perform a conditional write operation of new pixel data (c. 2, ll. 41-50). External depth data indicates distance between object on display screen and viewer (c. 2, ll. 34-39). Read, compare, and conditional write operations are performed during single clock cycle (c. 6, ll. 9-16). Fig. 6 shows 3rd clock cycle is clock cycle that starts performing read, compare, and conditional write operations during single clock cycle. So, depth-

compare write command is received from display processor responsive to 3rd of at least 7 clock cycles; receiving external depth data responsive to 3rd of at least 7 clock cycles, external depth data indicating distance between object on display screen and viewer; receiving at least one control signal from display processor responsive to 3rd of at least 7 clock cycles; comparing received external depth data with internal depth data stored in memory cell array of memory device, comparing being completed before one of 6th and 7th of 7 clock cycles. Since Ryherd teaches that the display processor controls the memory device (c. 8, ll. 23-26), and it is well-known in the art to use a memory controller to control the memory device, it would have been obvious to one of ordinary skill in the art to modify the device of Ryherd to include a memory controller so that the memory controlling operations that are performed by the display processor are instead performed by the memory controller.

25. As per Claim 33, Ryherd teaches replacing internal depth data with external depth data if external depth data is smaller than internal depth data, replacement occurring without modifying external depth data (c. 2, ll. 46-50; c. 5, ll. 54-68).

26. As per Claim 34, Ryherd teaches comparing and replacing are completed before one of sixth and seventh of seven clock cycles (Fig. 6; c. 2, ll. 41-50; c. 6, ll. 9-16).

27. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ryherd (US004970499A) in view of Dowdell (US005301263).

Ryherd is relied upon for the teachings as discussed above relative to Claim 34.

However, Ryherd does not teach at least one status signal is transmitted from memory device to memory controller, at least one status signal indicating whether internal depth data was replaced with external depth data, at least one status signal being transmitted responsive to one of

sixth and seventh of seven clock cycles. However, Dowdell teaches at least one status signal is transmitted from memory device to memory controller, at least one status signal indicating whether internal depth data was replaced with external depth data, and this is included in the read/compare/write operation (c. 8, ll. 12-39). Ryherd teaches read/compare/write operation is performed responsive to one of sixth and seventh of seven clock cycles, as shown in Fig. 6 (c. 2, ll. 41-50; c. 6, ll. 9-16). So, device of Ryherd can be modified to include the status signal of Dowdell to be transmitted responsive to one of sixth and seventh of seven clock cycles.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Ryherd so status signal is transmitted from memory device to memory controller, status signal indicating whether internal depth data was replaced with external depth data, at least one status signal being transmitted responsive to one of sixth and seventh of seven clock cycles because Dowdell suggests this is needed so memory controller knows when internal depth data was replaced with external depth data so memory controller knows when to retrieve new external depth data to send to processor for processing (c. 8, ll. 12-39).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

KEE M. TUNG
SUPERVISORY PATENT EXAMINER